ECE/COMPSCI 350L: Digital Systems

Course Information

Instructor:	Craig LaBoda	**Lecture:**	M/Tu/W/Th/F	1:00-2:15
Email:	craig.laboda@duke.edu	**Lab:**	M/Th	2:30-5:00
Office:	Hudson 217	**TA:**	Safkat Islam	
Hours:	W 2:30 – 3:30 pm	**Hours:**	Tu/F 11:00 am – 12:00 pm	

Course Description

This course teaches students the fundamentals of combinational and sequential logic design. Lectures will focus on the formalisms for building complex digital logic, beginning with simple building blocks and moving up the stack to larger systems. Lab exercises will reinforce lecture concepts with hands-on design assignments using a mix of programmable logic chips and dual-inline packages on breadboards. Students will learn how to write structural Verilog, and throughout the semester, build the individual components of a fully pipelined processor. This processor will then be applied towards a final group project, in which students will design and implement an in-depth system. Past examples of such projects include arcade games, cryptography systems, text editors, and audio synthesizers.

Objectives

The goal of this course is to teach students the following:

- Boolean algebra
- Combinational logic design
- Structural Verilog
- Boolean arithmetic (addition, subtraction, multiplication, and division)
- Memory elements and sequential logic design
- Implementation and minimization of finite-state machines
- Complementary metal-oxide-semiconductor (CMOS) logic design
- Five-stage pipelined processor design

Suggested Readings

Digital Design: A Systems Approach by Dally and Harting (ISBN: 9780521199506) is the recommended textbook; however, it is not required, i.e. assignments will not be taken directly from the book. Following the suggested reading is strongly encouraged!

Grading

Homework	30%	(750 points)
Labs	15%	(375 points)
Midterm	10%	(250 points)
Final Project	25%	(625 points)
Final Exam	20%	(500 points)

Assignments will be accepted up to 1 week after the due date. Late assignments will be deducted 10% per day. Students should not work together on assignments (see Academic Integrity section below). Homework regrades will only be considered for one week following grade posting.

Lab Expectations

Labs may run over the allotted time slot. For this reason, two separate days have been dedicated to the longer lab assignments. If students still cannot finish within the lab time slots, they are expected to arrange additional time with the lab TA to finish the assignment. Labs will be graded solely based on completion and working demonstrations.

Academic Integrity

Students are expected to uphold the Duke Community Standard:

> "Duke University is a community dedicated to scholarship, leadership, and service and to the principles of honesty, fairness, respect, and accountability. Citizens of this community commit to reflect upon and uphold these principles in all academic and non-academic endeavors, and to protect and promote a culture of integrity.
>
> To uphold the Duke Community Standard:
>
> I will not lie, cheat, or steal in my academic endeavors;
> I will conduct myself honorably in all my endeavors; and
> I will act if the Standard is compromised."

Students are allowed to ask one another questions but are expected to work alone on homework assignments unless directly told otherwise. Students caught violating the Duke Community Standard will be reported to the Office of Student Conduct. Note that programming submissions will be compared to one another using Stanford's Measure of Software Similarity (MOSS) to detect signs of plagiarism. You have been warned!

Course Outline

Week	Date	Lecture	Reading	Lab	Open	Due
1	5/18	Intro/Boolean Algebra			HW 1	
1	5/19	Logic Blocks	1, 2, 3			
1	5/20	Logic Blocks/Verilog	7, 8		HW 2	
2	5/23	Verilog	15.2	Lab 0 – Introduction		HW 1
2	5/24	Verilog and Registers				
2	5/25	Signed Arithmetic	10, 12			
2	5/26	Fast Adders and ALUs		Lab 1 – RCA	HW 3	
2	5/27	Multiplication				HW 2
3	5/30	NO CLASS				
3	5/31	Booth's Alg. and Div.		Lab 2 – Comparators		
3	6/1	Memory Elements	14,15,27		HW 4	
3	6/2	Factorization	6	Lab 3 – Memory		
3	6/3	Midterm Review				HW 3
4	6/6	Midterm				
4	6/7	Factorization				
4	6/8	Quine-McCluskey				
4	6/9	Pipelining	23, 24		HW 5	
4	6/10	Pipelining				HW 4
5	6/13	Pipelining/FSMs	16, 17	Lab 4/Projects – FSMs		
5	6/14	FSMs				
5	6/15	FSMs				
5	6/16	FSM Minimization		Project Proposals		
5	6/17	FSMs/CMOS Design	4, 5			
6	6/20	CMOS Design				HW 5
6	6/21	Defect Tolerance				
6	6/22	Testing	20			
6	6/23	Hazards/Gate Arrays	8.10			
6	6/24	Final Exam Review				
7	6/27	Project Demonstrations				
7	6/29	Final Exam				